Curriculum Vitae

Antonia Zhai

June, 2010

Home Address:
20 2nd St. NE, Apt 1609
Minneapolis, MN, USA, 55413

Webpage: http://www.cs.umn.edu/∼zhai
Email: zhai@cs.umn.edu

Office Address:
Department of Comp. Sci. & Eng.
University of Minnesota
4-198 EE/CSci Building
Minneapolis, MN, USA, 55455

Academic History

Current Position

Assistant Professor University of Minnesota, Minneapolis, MN, Jan. 13th, 2005

Education

Ph.D. Computer Science,
Carnegie Mellon University, Pittsburgh, PA, 1998 - 2005
Thesis: Compiler Optimizations for Thread-Level Speculation Execution
Advisor: Todd C. Mowry

M.A.Sc. Computer Engineering,
University of Toronto, Toronto, Canada, 1996 - 1998
Thesis: Benefits of Code Motion on TLDS Architecture for Non-Numerical Applications
Advisor: Todd C. Mowry

B.A.Sc University of Toronto, Toronto, Canada, 1992-1996

Award

- IBM Faculty Award, *"Hardware and Software Support for Flexible and Scalable Speculative-Parallel-Execution Models on Multicore Processors"*, 2007
- Best paper award, Venkatesan Packirisamy, Antonia Zhai and Pen-Chung Yew, *"Performance and Power Comparison of Thread-Level Speculation in SMT and CMP Architectures"*, in the Proc. The International Conference of Computer Design (ICCD), Lake Tahoe, CA, Oct 12, 2008

Funding:

Externally Funded

- NSF. *CPS:Medium: Embedded Fault Detection for Low-Cost, Safety-Critical Systems*, (PI: Gary Balas; co-PIs: Jaideep Srivastava, Mats Heimdahl and Antonia Zhai) $1,500,000.00, (09/01/09 - 08/31/2011)
- NSF. *SHF:Small:In Vivo Software Monitoring: Architectural and Compiler Support*, (PI: Antonia Zhai; co-PI: Mats Heimdahl) $499,271, (09/01/09 - 08/31/2011)
- NSF. *CSR-PSCE,TM: Dynamic Runtime Optimization and Adaptation for High Performance and Power Management on Multi-Core Processors*, (PI: Antonia Zhai; co-PIs: Wei-Chung Hsu and Pen-Chung Yew (Prof. Hsu was the PI at the time of application) $360,000, (09/01/08 - 08/31/2010) with
- Semiconductor Research Corporation (SRC). *Integrated Layout and Architectural Design for Multicore Platforms*, (PI: Sachin Sapatnekar; co-PI: Antonia Zhai) $330,000, (07/01/08 - 06/30/10) (Equal Contribution).
- IBM Faculty Award. *Hardware and Software Support for Flexible and Scalable Speculative-Parallel-Execution Models on Multicore Processors*, $20,000, 2007

Internally Funded

- Grant-in-Aid, University of Minnesota. *Architectural Design Innovations with 3D Die Stacking*, $25,412, (01/01/2008 - 06/30/2009)
- Grant-in-Aid, University of Minnesota. *Supporting In-vivo Monitoring on Multi-Core Processors*, $22,924, 06/01/2006 - 05/31/2007

In Submission:

- NSF. *SHF:Small:Dynamically Deploy Performance-Enhancing Threads in Multicore Systems*, (PI: Antonia Zhai) 2009

Publications and Scholarly Addresses:

Refereed Journals

1. Antonia Zhai, J. Gregory Steffan, Christopher B. Colohan, and Todd C. Mowry, *"Compiler and Hardware Support for Reducing the Synchronization of Speculative Threads"*, ACM Transactions on Architecture and Code Optimization, Volume 5, Issue 1, Pages 2-34, April 2008. (Major Contribution)
2. J. Gregory Steffan, Christopher B. Colohan, Antonia Zhai and Todd C. Mowry, *"The STAMPede Approach to Thread-Level Speculation"*, ACM Transactions on Computer Systems (TOCS), Volume 23, Issue 3, Pages 253 - 300, August 2005. (Minor Contribution)

Refereed Journals (Submitted)

1. Guojin He and Antonia Zhai. *"Efficient Dynamic Program Monitoring on Multi-Core Systems"*, **Submitted**

2. Yangchun Luo and Antonia Zhai. *"Dynamic Performance Tuning for Speculative Threads"*, **Submitted**

3. Antonia Zhai and Venkatesan Packirisamy. *"Energy Efficiency of Speculative Threads"*, **Submitted**

4. Antonia Zhai and Shengyue Wang. *"Compiler Optimizations for Speculative Threads in General-Purpose Applications"*, **Submitted**

Highly Selective Conferences

1. Yangchun Luo, Venkatesan Packirisamy, Wei-Chung Hsu and Antonia Zhai *"Energy-Efficient Speculative Threads: Dynamic Thread Allocation in Same-ISA Heterogeneous Multicore System"*, in the Proc. the Parallel Architectures and Compilation Techniques (PACT), 2010. (Acceptance Rate: 17%) (Major Contributor: 90% among faculty)

2. Guojin He and Antonia Zhai, *"Improving the Performance of Program Monitors with Compiler Support in Multi-Core Systems"*, in the Proc. the IEEE International Parallel & Distributed Processing Symposium (IPDPS), 2010. (Acceptance Rate: 24%) (Major Contributor: 100% among faculty)

3. Yangchun Luo, Venkatesan Packirisamy, Wei-Chung Hsu, Antonia Zhai, Nikhil Mungre, Ankit Tarkas. *"Dynamic Performance Tuning for Speculative Threads"*, in the Proc. International Symposium on Computer Architecture (ISCA), 2009 (Acceptance Rate: 20%) (Major Contribution: 80% among faculty)

4. Venkatesan Packirisamy, Antonia Zhai, Wei-Chung Hsu, Pen-Chung Yew, and Tin-Fook Ngai. *"Exploring speculative parallelism in SPEC2006"* in the Proc. IEEE International Symposium on Performance Analysis of Systems and Software (ISPASS), 2009 (Acceptance Rate: 28%) (Major Contribution: 80% among faculty)

5. Venkatesan Packirisamy, Antonia Zhai and Pen-Chung Yew, *"Performance and Power Comparison of Thread-Level Speculation in SMT and CMP Architectures"*, in the Proc. The International Conference of Computer Design (ICCD), Lake Tahoe, CA, Oct 12, 2008 **(Best Paper)** (Acceptance Rate: 34%) (Major Contribution: 80% among faculty)

6. Xiaoru Dai, Antonia Zhai, Wei-Chung Hsu and Pen-Chung Yew, *"A General Compiler Framework for Speculative Optimizations Using Data Speculative Code Motion"*, in the Proc. 2005 International Symposium on Code Generation and Optimization (CGO-2005) San Jose, CA, USA, March 20-23, 2005. (Acceptance Rate: 35%) (About equal contribution: 50% among faculty)

7. Antonia Zhai, Christopher B. Colohan, J. Gregory Steffan and Todd C. Mowry, *"Compiler Optimization of Memory-Resident Value Communication Between Speculative Threads"*, in the Proc. 2004 International Symposium on Code Generation and Optimization (CGO-2004), Palo Alto, CA, USA, March 20-24, 2004. (Acceptance Rate: 32%) (Major Contribution: 80% among students)

8. Antonia Zhai, Christopher B. Colohan, J. Gregory Steffan and Todd C. Mowry, *"Compiler Optimization of Scalar Value Communication Between Speculative Threads"*, in the Proc. The Tenth International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS-X), San Jose, CA, USA, Oct 7-9, 2002. (Acceptance Rate: 14%) (Major Contribution: 80% among students)

9. J. Gregory Steffan, Christopher B. Colohan, Antonia Zhai and Todd C. Mowry, *"Improving Value Communication for Thread-Level Speculation"*, in the Proc. the Eighth International Symposium on High Performance Computer Architecture (HPCA'02), Cambridge, MA, Feb 2002. (Acceptance Rate: 20%) (Minor Contribution: 30% among students)

10. J. Gregory Steffan, Christopher B. Colohan, Antonia Zhai and Todd C. Mowry, *"A Scalable Approach to Thread-Level Speculation"*, in the Proc. International Symposium on Computer Architecture 2000 (ISCA'00), Vancouver, Canada, June 2000. (Acceptance Rate: 17%) (Minor Contribution: 20% among students)

Other Referred Conferences/Workshops

1. Vineeth Mekkat, Ragavendra Natarajan, Wei-Chung Hsu and Antonia Zhai, *Performance Characterization of Data Mining Benchmarks* The Fourteenth Workshop on Interaction between Compilers and Computer Architectures (Interact-14), Pittsburgh, PA, March 13, 2010. (Major Contribution: 80% among faculty)

2. Antonia Zhai, Shengyue Wang, Pen-Chung Yew, and Guojin He, *"Compiler Optimizations for Parallelizing General-Purpose Applications under Thread-Level Speculation"*, poster in the 13th ACM SIGPLAN Symposium on Principles and Practice of Parallel Programming (PPoPP'08), Salt Lake City, Utah, February 20-23, 2008. (Presenter: Yangchun Luo) (Major Contribution: 80% among faculty)

3. Venkatesan Packirisamy and Antonia Zhai, *"Exploiting TLS Parallelism at Multiple Loop-Nest Levels"*, in the Proc. Fifteenth International Conference on Parallel and Distributed Systems (ICPADS), 2009 (Acceptance Rate: 28%) (Major Contribution: 80% among faculty)

4. Antonia Zhai, Guojin He, and Mats Heimdahl, *"Hardware and compiler support for dynamic software monitoring"*, in the Proc. 9th International Workshop on Runtime Verification (RV 2009), Grenoble, France, June, 2009 (Major Contribution: 80% among faculty)

5. Guojin He, Antonia Zhai, and Pen-Chung Yew, *"Ex-Mon: An Architectural Framework for Dynamic Program Monitoring on Multicore Processors"*, The Twelfth Workshop on Interaction between Compilers and Computer Architectures (Interact-12), Salt Lake City, Utah, February 16, 2008. (Major Contribution: 80% among faculty)

6. Venkatesan Packirisamy, Shengyue Wang, Antonia Zhai, Wei-Chung Hsu, and Pen-Chung Yew, *"Supporting Speculative Multithreading on Simultaneous Multithreaded Processors"*, in the Proc. International Conference on High Performance Computing (HiPC'06), Bangalore, India, December 18-21, 2006. (Acceptance Rate: 16%) (Major Contribution: 80% among faculty)

7. Shengyue Wang, Antonia Zhai, and Pen-Chung Yew, *"Exploiting Speculative Thread-Level Parallelism in Data Compression Applications"*, in the Proc. 19th International Workshop on Languages and Compilers for Parallel Computing (LCPC'06), New Orleans, Louisiana, November 2-4, 2006. (Major Contribution: 80% among faculty)

8. Rao Fu, Jiwei Lu, Antonia Zhai, and Wei-Chung Hsu, *"A Study of the Performance Potential for Dynamic Instruction Hints Selection"*, in the Proc. 11th Asia-Pacific Computer Systems Architecture Conference (ACSAC 2006), Shanghai, China, September 6-8, 2006. (Also published in "Advances in Computer Systems Architecture", Lecture Notes in Computer Science, Vol. 4186, Springer, ISBN: 3-540-40056-7) (Minor Contribution: 30% among faculty)

9. Abhinav Das, Antonia Zhai, Rao Fu, and Wei-Chung Hsu, *"Issues and Support for Dynamic Register Allocation"*, in the Proc. 11th Asia-Pacific Computer Systems Architecture Conference (ACSAC 2006), Shanghai, China, September 6-8, 2006. (Also published in "Advances in Computer Systems Architecture", Lecture Notes in Computer Science, Vol., 4186, Springer, ISBN: 3-540-40056-7) (Minor Contribution: 30% among faculty)

10. Shengyue Wang, Kiran S Yellajyosula, Antonia Zhai and Pen-Chung Yew, *"Loop Selection for Thread-Level Speculation"*, in the Proc. 18th International Workshop on Languages and Compilers for Parallel Computing (LCPC'05), Hawthorne, New York, USA, October 20-22, 2005. (Major Contribution: 80% among faculty)

Scholarly Addresses

1. *"Dynamic Tuning for Speculative Threads"*, Institute of Computing Technology, Beijing, June 2010

2. *"Dynamic Tuning for Speculative Threads"*, National Ciaotong University, Tsinchu, May 2010

3. *"Dynamic Performance Tuning for Speculative Threads"*, Cornell University, Ithaca, Oct. 2009

4. *"Dynamic Performance Tuning for Speculative Threads"*, IBM Research Lab, Yorktown Heights, Oct. 2009

5. *"Dynamic Performance Tuning for Speculative Threads"*, Intel Research Lab, Santa Clara, Oct. 2009

6. *"Exploiting the Potential of Multicore Processors"*, Academia Sinica, Taiwan, June, 2009

7. *"Exploiting the Potential of Multicore Processors"*, National Taiwan University, Taiwan, June, 2009

8. *"Exploiting the Potential of Multicore Processors"*, Institute of Computer Technology, Beijing, China, June, 2008

9. *"Exploiting the Potential of Multicore Processors"*, Tsinghua University, Beijing, China, June, 2008

10. *"Extracting Thread-Level Parallelism for Multi-Core Processors"*, T. J. Watson Lab, IBM, Yorktown Heights, NY, Jan, 2008.

11. *"Extracting Coarse-Grain Parallelism for Multi-Core Processors"*, Intel Corporation, Folsom, CA, Oct, 2007.

12. *"An Overview of Multi-Core Research at the CSE Dept in U of Minnesota"*, Honeywell International, Minneapolis, MN, Feb, 2007.

13. *"Compiler Optimization for Thread-Level Speculation"*, Microsoft Research in Silicon Valley, Mountain View, CA, Feb, 2005.

14. *"Compiler Optimization for Thread-Level Speculation"*, University of Pittsburgh, Pittsburgh, PA, Jan, 2005.

15. *"Compiler Optimization for Thread-Level Speculation"*, Massachusetts Microprocessor Design Center, Intel Boston, MA, Oct, 2004.

16. *"Compiler Optimization of Memory-Resident Value Communication Between Speculative Threads"*, 2004 International Symposium on Code Generation and Optimization (CGO-2004), Palo Alto, CA, March 20, 2004.

17. *"Compiler Optimization of Memory-Resident Value Communication Between Speculative Threads"*, Computer Architecture Lab at Carnegie Mellon (CALCM) Seminar, Pittsburgh, PA, Feb 10, 2004.

18. *"Compiler Optimization of Scalar Value Communication Between Speculative Threads"*, The Tenth International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS-X), San Jose, CA, Oct 8, 2002.

19. *"Compiler Optimization of Scalar Value Communication Between Speculative Threads"*, Computer Architecture Lab at Carnegie Mellon (CALCM) Seminar, Pittsburgh, PA, September 17, 2002.

Student Supervision

Student	Degree	Title/Topic	Graduation Date
Anup P Holey	Ph.D.	Thread-Management in Heterogeneous Multicore Systems	2014 (Expected)
Jieming Yin	Ph.D.	Multicore System Energy Efficiency: Interconnection and Floorplanning Perspective	2013 (Expected)
Vineeth Mekkat	Ph.D.	Improving Data Mining Applications in Multicore Systems	2012 (Expected)
Ragavendra Natarajan	Ph.D.	Dynamic Optimization for Data Mining Applications	2012 (Expected)
Yangchun Luo	Ph.D.	Dynamic Optimization of Speculative Execution	2011 (Expected)
Guojin He	Ph.D.	Architectural Support to Improve Software Programmability	2010 (Expected)
Venkatesan Packirisamy	Ph.D.	Exploring Efficient Architecture Design for Thread-Level Speculation— Power and Performance Perspective	2009
Shengyue Wang	Ph.D.	Extracting parallel threads from non-numeric applications	2007
Mohamed Suhail Ubaidur	M.S.	Experimenting with Heterogeneous Multicore Systems on GEMS	2010
Hwaseob Sim	M.S.	Identifying Dynamic Program Behaviors in Data Mining Applications	2010
Harish Barathvajasankar	M.S.	Implementing TLS Support for IA64-Based CMP	2006
Amitkumar K. Puthenveetil	M.S.	Implementing TLS for IA64-Based CMP Using the Liberty Simulation Environment	2005

- Shengyue Wang, Venkatesan Packirisamy are co-advised with Prof. Yew.

Courses Taught

Course Number	Course Title	Year	Class Size	Evaluation Q1	Q2	Q3	Q4	Q5	Q6
CSCI 8205 EE 8367	Parallel Machine Organization Organization	Spring 2009	19	5.27/6	5.18/6	5.09/6	5.55/6	5.55/6	5.45/6
CSCI 2021	Machine Architecture and Organization	Fall 2008	66	4.88/6	3.93/6	4.04/6	4.95/6	4.91/6	4.44/6
CSCI 8205 EE 8367	Parallel Machine Organization	Spring 2008	15	5.33/6	5.17/6	4.33/6	5.50/6	5.50/6	5.33/6
CSCI 5204 EE 5364	Advanced Computer Architecture	Fall 2007	44	5.7/7	6.2/7	6.2/7	6.2/7	5.5/7	N/A
CSCI 2021	Machine Architecture and Organization	Spring 2007	76	4.4/7	5.7/7	4.9/7	4.4/7	4.6/7	N/A
CSCI 5204 EE 5364	Advanced Computer Architecture Organization	Fall 2006	31	4.6/7	6.1/7	5.7/7	6.0/7	4.7/7	N/A
CSCI 5204 EE 5364	Advanced Computer Architecture	Fall 2005	34	3.6/7	5.2/7	4.4/7	4.6/7	3.6/7	N/A
CSCI 5980	Current Trends in Computer Architecture and Compiler Optimization	Spring 2005	4	6.0/7	6.0/7	7.0/7	7.0/7	6.5/7	N/A

Ph.D Thesis Committees

Thesis Defense Served and Completed

- Qunzeng Liu, , 2010
- Jing Wang, *Optimized MIMO Channel Allocation in Software-Defined Radio*, 2009
- Anand Singh, *A Framework for Optimizing Risks to Information*, 2009
- Kichul Chun, *Embedded Memory Circuit Design in Nanoscale Technology*, 2009
- Tony Tae-Hyoung Kim, *Design Techniques for Ultra-low Voltage Sub-threshold Circuits and On-chip Reliability Monitoring*, 2009
- Myung-Hwan Park, *An Approach for Oracle Data Selection*, 2009
- Fakhrul Zaman Rokhani, *Low Power Design of Bus Communication*, 2008

- Manho Kim, *On-chip communication performance improvement by using network technology*, 2007
- Abhinav Das, *Techniques for Improving Dynamic Binary Optimization*, 2007
- Chao Cheng, *High-Speed Low-Cost VLSI DSP Algorithms Based on Novel Fast Convolutions and Look-Ahead Pipelining Structures*, 2007
- Brent Goplen, *Advanced Placement Techniques for Future VLSI Circuits*, 2006
- Daewook Kim, *Packet Switched Scalable On-Chip Interconnection Architecture Design and Implementation for Networks-on-Chip*, 2006
- Jiwei Lu, *Design and Implementation of a Lightweight Runtime Optimization System on Modern Computer Architectures*, 2006

Prelim Oral Served
John Keane (2010); Pingqiang Zhou (2010); Yaoguang Wei (2010); Pei-Hung Lin (2009); Jagan Jayaraj (2009); Woojoon Lee (2009).

Professional Activities

Professional Societies

- Member of the Institute of Electrical and Electronics Engineers (IEEE)
- Member of the Association of Computing Machinery (ACM)

Conference/Workshop Organization and Committee

- Program Committee:
  - The International Conference on Parallel Processing (ICPP), 2011
  - ACM SIGPLAN Symposium on Principles and Practice of Parallel Programming (PPoPP), 2011
  - Workshop on Interaction between Compilers and Computer Architectures (INTERACT), 2010
  - International Symposium on Low Power Electronics and Design (ISLPED), 2010
  - International Conference on Parallel Architecture and Compilation Techniques (PACT), 2008
  - Workshop on Parallel Execution of Sequential Programs on Multi-core Architectures (PESPMA), 2008
  - ACM SIGPLAN Symposium on Principles and Practice of Parallel Programming (PPoPP), 2008
  - International Conference on Parallel and Distributed Systems (ICPADS), 2007
  - Workshop on Interaction between Compilers and Computer Architectures (INTERACT), 2005
- Local Arrangement Chair: 12th International Conference on Parallel and Distributed Systems (ICPADS), 2006

Conference and Journal Reviewed

- Journals Reviewed:
  - Journal of Information Science and Engineering (JISE)
  - ACM Transactions on Architecture and Code Optimization(TACO)
  - ACM Transactions on Computer Systems (TOCS)
  - IEEE Transactions on VLSI Systems
- Conferences and Workshops Reviewed:
  - Extermal review committee for Architectural Support for Programming Lanaguage and Operating Systems (ASPLOS), 2011
  - Workshop on Interaction between Compilers and Computer Architectures (INTERACT), 2010
  - International conference on High-Performance Embedded Architectures and Compilers (HiPEAC) 2009
  - IEEE/ACM International Symposium on Microarchitecture (MICRO) 2009
  - International Symposium on Programming Language Design and Implementation (PLDI-2008), 2008
  - International Symposium on Computer Architecture (ISCA-2008), 2008
  - International Symposium on Code Generation and Optimization (CGO-2007), 2007
  - The 39th Annual IEEE/ACM International Symposium on Microarchitecture (MICRO-39), 2006
  - 12th International Symposium on High Performance Computer Architecture (HPCA),2006
  - 10th Asia-Pacific Computer Systems Architecture Conference (ACSAC), 2005
  - 9th Annual Workshop on Interaction between Compilers and Computer Architectures (INTERACT-9), 2005
  - IEEE International Symposium on Performance Analysis of Systems and Software, 2005 (ISPASS)
- Proposal Reviewed
  - NSF Panel (2008)

University Committee Work and Other Activities

- Served on Computing Committee, CSE Dept, University of Minnesota, 2009 - 2010
- Served on WPE Committee, CSE Dept, University of Minnesota, 2008 - 2009
- Organized the HPCC seminar series, CSE Dept, University of Minnesota, Fall 2004, Spring 2005, Spring 2006, Fall 2007, Spring 2008,
- Served on Curriculum Committee, CSE Dept, University of Minnesota, 2007-2008,
- Served on graduate school Admission Committee, CSE Dept, University of Minnesota, 2005, 2006,
- Served on graduate school Admission Committee, CS Dept, Carnegie Mellon University, 2000,