Summary
A systematic methodology to compute the architectural vulnerability factors for a high performance microprocessor.

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1 To be completed before class

What are the problems solved by this paper? (50 words)

With reducing transistor size, the errors due to particle sizes is becoming prominent. Techniques to deal with these errors require accurate error estimates to design processors with appropriate cost/reliability tradeoffs.

What are the approaches attempted by this paper? (50 words)

The authors introduce a metric called AVF to assess the reliability of the processor. They propose schemes to reduce the number of components to track by defining ACE and un-ACE bits. They identify various hardware bits and software instructions which do not effect the correctness of the output and propose a method to compute the upper-bound on the AVF.

What are the main conclusions of this paper? (50 words)

The authors propose and implement a scheme to identify bits in the pipeline that might cause errors in the processor pipeline. They computed the AVF for the instruction queue and the execution units of an IA64 processor. They suggest to improve the reliability of the ACE bits to improve the reliability of the processor.

2 To be completed after class

Did this paper address an important issue? Explain. (100 words)

This paper proposes a metric AVF that can be used to estimate the reliability of a component or chip and thereby help focus design and test time to improve on the reliability of the component. It also helps reduce the money spent in redundancy to the critical components.

The paper also proposes how to compute the AVF for components(bits) which hold critical information only for a percentage of the execution time. Thie paper further proposes ACE bits which are used for maintaining architecturally correct state while execution. The authors then use their technique to estimate the AVF for critical components in the processor as the instruction queue and execution unit.

Are the proposed approaches valid? Describe its strength and weakness. (100 words)

The approach is an estimation technique for predicting the reliability of a processor. The authors assume that all the bits in the processor are ACE bits until proved otherwise. This method ensures that none of the components are missed out. This provides designers a good hint towards the component to spend the design effort on.

There may be a great number of ACE bits due to the assumption that all processor bits are ACE bits. The authors compute the AVF using the percentage of time the bit holds vital bits. This approach
depends on the program being run on the processor, thereby leading to isolation of a few components. This approach doesn’t handle errors induced to interfacing the processor with other off-chip components.

Do the results support the conclusions? Explain. (100 words)

The authors analyse the hardware based on the composition of the instructions in the SPEC integer and floating point programs and found that ACE instructions comprised of 45% of the instructions executed. The authors observed that the average IPC for the ACE instructions to be 0.45 for integer programs and 0.77 for floating point programs, which was attributed to the high predictability of floating point programs. They also traced the number of cycles during which a processor has ACE instructions.

Describe the potential future works? (100 words)

The authors can extend the work to all the components in the processor and compute the AVF for all the pipeline stages. The authors can extend the metric to compute the errors induced due to interfacing with other processors, by treating the network interface like hardware bits. The authors can extend their method of detecting un-ACE bits by tracking other instructions of no consequence.