Summary
Razor: A Low-Power pipeline based on circuit level timing speculation
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1 To be completed before class

What are the problems solved by this paper? (50 words)
Dynamic voltage scaling is a commonly used technique to reduce power. But we cannot reduce power indefinitely since, we need a critical supply voltage to ensure correct execution. But the circuit can run at a much lower voltage that this and the critical voltage is needed only under some rare data patterns. So if we can recover from errors, we can run the pipeline at a much lower voltage.

What are the approaches attempted by this paper? (50 words)
This paper proposes architectural and circuit level techniques to use sub-critical voltages to run the pipeline. The pipeline detects the error rate and accordingly adjusts the voltage. To ensure correct execution, a shadow latch is kept for each flip flop. If a error is detected the value from the latch is fed to the next stage in the pipeline.

What are the main conclusions of this paper? (50 words)
The razor technique proposed was implemented in a prototype 64-bit alpha processor design. Circuit analysis of a FPGA multiplier showed a 17% reduction in energy. Architectural simulations showed a decrease of only 2.5% in pipeline throughput. So from the data it seems that razor is an effective technique of reducing power consumption while keeping the performance lose to a minimum.

2 To be completed after class

Did this paper address an important issue? Explain. (100 words)

Are the proposed approaches valid? Describe its strength and weakness. (100 words)

Do the results support the conclusions? Explain. (100 words)

Describe the potential future works? (100 words)