

# Summary

## Drowsy Caches: Simple Techniques for Reducing Leakage Power

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### 1 To be completed before class

**What are the problems solved by this paper? (50 words)**

Leakage current is set to dominate the total power consumption of a processor and caches are one of the most important source of leakage. Only a small part of the cache is accessed at a time and all the remaining parts remain idle but at the same time consuming power.

**What are the approaches attempted by this paper? (50 words)**

One approach is to gate the parts of the unused cache. But this means that we lose the data and hence have to go to the memory to get this data. In this paper the cache is not switched off, instead it is put in a drowsy state where it uses a reduced voltage. When we want to read the data from a drowsy line, we have to bring the line to active state (takes 1 or 2 cycles) and then read from it. So this is much better than gating off the cache. Also simple techniques of turning all cache to drowsy at regular intervals seems to be good technique.

**What are the main conclusions of this paper? (50 words)**

Simple drowsy cache technique can reduce the cache power consumption by 80%. Due to the small working set in most of the benchmarks, very simple techniques could give very huge power reduction. Though this might not be true if we consider other benchmarks. When static power is reduced by such huge amounts the dynamic power could become a major issue.

### 2 To be completed after class

**Did this paper address an important issue? Explain. (100 words)**

**Are the proposed approaches valid? Describe its strength and weakness. (100 words)**

**Do the results support the conclusions? Explain. (100 words)**

**Describe the potential future works? (100 words)**