Summary Part 1
Razor: A Low-Power Pipeline Based on Circuit-Level Timing Speculation

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What are the problems solved by this paper?
Several techniques have been proposed to reduce the power consumption in a circuit by reducing the operating voltage and frequency. However, most of these techniques have to provide some conservative margins for the (voltage,frequency) values to ensure that the circuit performs correctly even under worst-case conditions. This paper proposes a solution by which the circuit can be operated even below the ‘critical’ voltage, so that no margins are required and thus more energy can be saved.

What are the approaches attempted by this paper?
The basic observation is that the worst-case conditions occur very rarely and depend upon the data being processed, among several other factors. So we can eliminate the ‘margins’ that are usually provided. This can lead to some errors when the worst-case conditions do occur (mostly due to data patterns). If these errors are detected and corrected, energy savings can be achieved without severe performance loss. To detect errors, a simple mechanism called ‘shadow latch’ is provided in a flip-flop (called Razor flip-flop). Metastability issues are also considered. The error rate is used to dynamically adjust the operating voltage so that the energy savings are maximized, while the performance loss is kept at a minimum.

What are the main conclusions of this paper?
The main findings are that the operating voltage can be reduced below the ‘conservative’ values, since the worst-case conditions do not occur frequently. The optimal voltage varies from program to program and even during program phases. Thus, having a DVS mechanism is more beneficial, since it can adapt itself to most program’s energy requirements while providing energy savings of more than 40%. Overall, the Razor approach is very effective at reducing the power consumption, while minimizing performance loss.