Summary
Razor: A Low-Power Pipeline Based on Circuit-Level Timing Speculation
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1 To be completed before class

What are the problems solved by this paper? (50 words) The supply voltage of a processor is reduced so as to reduce the power consumption such that the program executes correctly in spite of environmental and process related variations and noises. This only allows a very conservative reduction in the supply voltage.

What are the approaches attempted by this paper? (50 words) The authors propose dynamic error detection and correction hardware in speed paths. They introduce Razor Flip-flops in the pipeline which uses a delayed clock to detect errors. The shadow latches in the flip-flops always have the correct states. The authors then discuss techniques of correcting error states in the pipeline by either introducing a pipeline stall with an additional pipeline stage (clock gating) or by flushing the pipeline (recovery using counterflow pipelining).

What are the main conclusions of this paper? (50 words)
Razor increases the pipeline energy by 3.1% compared to a non-Razor design of the architecture. Decreasing the voltage to point where 1.5% of the operations fail reduces energy consumption by 35%.

2 To be completed after class

Did this paper address an important issue? Explain. (100 words)

Are the proposed approaches valid? Describe its strength and weakness. (100 words)

Do the results support the conclusions? Explain. (100 words)

Describe the potential future works? (100 words)