Summary
Continual Flow Pipelines
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1 To be completed before class

What are the problems solved by this paper? (50 words)
The paper addresses the costs associated with achieving performance by increasing the size of the instruction window, number of registers and commit buffer. Each of the above complicates the logic involved and increases the associated cost in terms of die size and power consumption.

What are the approaches attempted by this paper? (50 words)
CFP proposes to implement a non-blocking pipeline architecture which moves loads causing cache-misses and instructions depending on the loads out into a Slice Processing Unit and thereby freeing the resources consumed by these instructions. The SPU then reintroduces these instructions into the pipeline once the load value returns.

What are the main conclusions of this paper? (50 words)
The paper proposes a non-blocking architecture which reduces the hardware resources required and has better performance than larger ROBs and CPR cores. The CFP can tolerate longer cache latencies and places less restrictions on the size of the cache required.

2 To be completed after class

Did this paper address an important issue? Explain. (100 words)
This paper proposes an architecture that produces high performance with small instruction windows and register sets inspite of the presence of long latency loads. The processor proposes to free the resources held by the operations dependent on the miss, there by allowing the processor to lookahead and prefetch data. This further helps reduce the size of the required caches and may reduce the size of the dye. The processor has a Slice Processing Unit which buffers instructions dependent on the long latency operations and values required by these instructions. The SPU reinserts these operations in data dependent order and uses a physical to physical addressing map.

Are the proposed approaches valid? Describe its strength and weakness. (100 words)
Strengths:

- The processor has better performance than most of the current ROB and CPR processors.
- The processor uses less register and instruction window resources.
- The processor requires less cache than the conventional ROB.
- The processor may consume less power due to decrease in required resources and may be build with lower cost due to the dye size.
- The processor depends only on branch prediction which is quite advanced. Advanced branch predictors predict at an accuracy of about 97%.
Weaken:
- The SPU is a complicated hardware which needs to be inserted into core.
- The physical to physical register map has to be implemented and tested.
- The processor proposes new paradigm in execution there by requiring the hardware to be tested exhaustively.

Do the results support the conclusions? Explain. (100 words)

The processor clearly outperforms ROB and CRP processors for a range of applications as can be observed from the speedup. The authors show the requirement of a better scheduler to improve the performance in Figure 2. Figure 6 depicts that the CFP has over 1000 instructions in flight over 40% of the execution time and also that the number of instructions entering the SPU is less than 10%. The authors further compare and show that CFP outperforms CPR processors with runahead execution and then compute the performance achievable with perfect branch prediction. The authors then compare the speedups achievable by CFPs over ROB based processors for different L2 cache sizes.

Describe the potential future works? (100 words)

The processor can be used as a single core in a multi-core processor and the performance can be studied. A comparison between multi-threaded applications and CFP is not clear, i.e., performance of CFP with a hyper-threading processor or a SMT processor is not yet clear. The power consumed by the processor is estimated to be lesser but there is no realistic data proposed in the paper. The authors do not discuss the working of the CFP when the clock speed is reduced.