Summary
Continual Flow Pipelines

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1 To be completed before class

What are the problems solved by this paper? (50 words)
Conventional superscalar processors relied on large instruction windows to extract instruction level parallelism. But these large instruction windows are not scalable leading to many design complexities and power wastage. We need such large windows to hold large number of instructions, so if any earlier instructions gets held up due to long latency operations, we can get other independent instructions to execute. But as the memory and CPU performance gap increasing, solution of using large windows in not efficient. This paper uses smaller windows but can tolerate long latency cache misses.

What are the approaches attempted by this paper? (50 words)
Continual flow pipelines allows processors to execute instructions after the long latency cache miss that are independent of the miss instruction. All the instructions that are dependent on the load is put into a Slice data buffer. The register mappings are properly handled in such a way that the following instructions will be able to execute as usual. When the load instruction completes, the instructions in the buffer are also committed. Thus we can still extract ILP beyond cache misses.

What are the main conclusions of this paper? (50 words)
With Continual flow pipelines we are able to tolerate the cache misses with a much smaller instruction windows than the conventional ROB based architectures. The CFP technique is found to be more effective than the CPR technique aimed at tolerating low confidence branches. After applying CFP, the branch mis-predictions have become the major bottleneck.

2 To be completed after class

Did this paper address an important issue? Explain. (100 words)

Are the proposed approaches valid? Describe its strength and weakness. (100 words)

Do the results support the conclusions? Explain. (100 words)

Describe the potential future works? (100 words)