

Venkatesan Packirisamy
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Education:

- PhD student - Dept. of Computer Science, University of Minnesota, Twin Cities
Sept-2003 – present
GPA - **3.975**
- B.E. - College of Engineering, Guindy, Anna University, Chennai, India
Aug. 1998 – Jun 2002
GPA – **8.8/10**

Current Research:

- Working on efficient implementation of Speculative multithreading in multi-core (CMP) and Simultaneous multithreading (SMT) processors.
- Developed a simulator to simulate speculative multithreading on CMP and SMT processors.
- Developed an efficient cache based algorithm for speculative multithreading in SMT processors.
- Comparing CMP and SMT for speculative multithreading, in terms of performance, power and temperature.

Experience:

Research Assistant:

Under Prof. Pen-Chung Yew, University of Minnesota, Minneapolis (Sep. 2003 – present).

Internships:

1. June 2006 – August 2006 - **Intel** (Advanced computing center, KAI labs, under Bob Kuhn)

Designed and implemented a linux based distributed file system for home environment. The Distributed Parallel Storage (DPS) system helps home users to better manage disk space and digital content.

2. June 2005 – August 2005 - **Intel** (Programming Systems Lab, under Roy Ju)

Understanding the performance impact of packet ordering in network processors. Involved modifying the code generated by Shangri-La compiler to enforce packet ordering.

3. June 2004-August 2004 - **Intel** (Programming Systems Lab, under Roy Ju)

Built a simulator for a Speculative Parallel threading architecture by modifying an IA32 simulator (iasim). The work involved designing a speculative multithreading architecture and implementing it in the iasim simulator.

Programmer Analyst:

July 2002 – Jun 2003 - Cognizant Technology Solutions, Chennai, India
Worked in the maintenance and enhancement of Online and Batch systems in IBM mainframes.

Publications:

1. Venkatesan Packirisamy, Shengyue Wang, Antonia Zhai, Wei-Chung Hsu and Pen-Chung Yew, "Supporting Speculative Multithreading on Simultaneous Multithreaded Processors" 13th Annual IEEE International Conference on High Performance Computing (HiPC 2006), December, 2006

2. Poster titled "*hardware assisted profile collection and reuse*", presented at the 8th international conference of High performance computing (HiPC 2001) held at Hyderabad, India

Undergraduate Research:

"*Hardware assisted profile collection and reuse in Chip multiprocessors*" – Execution profile of programs is collected and stored along with the executable. This profile is used to improve performance for subsequent executions.

Skill Set:

Programming knowledge: C, C++, C#, OpenMP, MPI, UPC, Java (J2EE), SQL, prolog, COBOL, JCL, REXX, CICS, Unix Shell
Programming, MPI programming
Operating Systems: Linux, Windows, IBM 390(MVS).
Databases: Oracle 8i, DB2, VSAM
Tools & Utilities: *ORC – Open Research Compiler, PIN – instrumentation tool for Itanium, SimpleScalar toolkit*, IBM mainframe Utilities, Lex and bison (compiler building tools).

Academic projects:

1. Improving power and reliability by reducing parallelism under cache miss – implemented using WATCH simulator.
2. Evaluation of analytical modeling of performance for parallel programs (SPEC openMP programs were studied)
3. Extracting Speculative Parallelism – characteristics of major loops in SPEC2000 integer benchmarks were studied and OpenMP like user directives were inserted to exploit speculative parallelism.
4. Data Prefetching for pointer intensive code – Implemented a greedy algorithm to prefetch data for irregular pointer accesses in the ORC compiler.
5. Study of correlated hardware prefetching techniques – different hardware prefetching techniques were implemented and studied using simpleScalar.

Work Status:

International Student holding F1 Visa. Citizenship – India